Vokasi Unesa Bulletin of Engineering, Technology and Applied Science (VUBETA)
https://journal.unesa.ac.id/index.php/vubeta
Vol. 2, No. 2, 2025, pp. 252~269 DOI: 10.26740/vubeta.v2i2.37801
ISSN: 3064-0768

Design of a Class AB Power Amplifier For 5G Applications

Joshua Aa-Daaryeb Nounyah[1], Bernice Ansu Pormaa[2], Emmanuel Mensah[3], Abdul-Rahman Ahmed[4], Raymond Gyang[5*]
[1,2,3,4,5] Department of Telecommunication Engineering, Kwame Nkrumah University of Science and Technology, Kumasi, Ghana
[5] Department of Electrical and Electronics Engineering, Bolgatanga Technical University, Bolgatanga, Ghana

Article Info

Article history:

Received January 03, 2025
Revised April 10, 2025
Accepted May 15, 2025

Keywords:

Class-AB operation
Efficiency
Linearity
Power amplifier
GaN HEMT
Power added efficiency
Small signal gain

ABSTRACT

This work discusses the utilization of GaN HEMT technology on Rogers substrate in the design as well as the analysis of a 200 MHz Class AB power amplifier (PA) tailored for use in the 5G sub 6 GHz frequency band, specifically targeting 2.4 GHz applications. This is to satisfy the efficiency and linearity constraints in typical 5G communications systems, especially at the input part of the communication chain, whiles realizing all round practical Figure of Merits (FoMs). Matching networks were devised employing cascaded L-section microstrip transmission lines, meticulously optimized for optimum output power, return loss, and PAE. This demonstrates the effectiveness of the design approach in producing substantial power with heightened efficiency. Furthermore, the design exhibited enhanced linearity, even in the absence of commonly utilized feedback networks such as voltage dividers or emitter/source degeneration due to the inherent robustness of the proposed design. The PA's performance aligned exceptionally well with theoretical predictions. Electromagnetic simulation results showed a small signal gain of 13.634 dB with return losses maintaining below -12 dB across the desired operational bandwidth. Also, a power output of 40.052 dBm for a 29 dBm input power was obtained, coupled with a PAE of 54.148%.

1. INTRODUCTION

In recent years, the necessity for transmitters in the communication block to be able to provide high-speed transmission over wide distances has grown. This is particularly so due to the launch of the 5G wireless communication technology [1][2] which has resulted in dramatic breakthroughs in mobile networks, allowing for high data rates, minimal latency, and improved connection [3]-[13]. However, the deployment of the 5G network brings with it a new set of obstacles, notably in the design and operation of power amplifiers (PAs), which are critical in guaranteeing effective signal transmission and reception [14]-[21]. The transmitters in 5G systems run at higher frequencies and use complicated modulation techniques, necessitating creative solutions [15]-[21][22]. One main component in transmitters that defines its overall performance is the power amplifier which is typically placed at the transmitter's last stage before transmission occurs [5][7][23]-[25]. The PA's output power, bandwidth, and linearity are key in the determination of the quality of communication networks while the efficiency shows the power consumption of the transmitter system and hence its reliability [10]-[12] [25]-[29].

Linearity characteristics showcased by power amplifiers in the presence of wideband input signals and high peak-to-average power ratios (PAPR) that define 5G waveforms, in particular, is one of the key problems [30]-[34]. Linear amplification is required to reduce distortion and spectrum regrowth, which can result in interference and poor signal quality [18]-[21]. Furthermore, the rising need for energy efficiency necessitates that power amplifiers perform at high efficiency even under variable load situations [3]-[8].

*Corresponding Author
Email: rgaang@bolgatu.edu.gh

Furthermore, because multiple-input multiple-output (MIMO) techniques are being used in 5G systems, power amplifiers must address the challenges associated with envelope tracking, envelope elimination and restoration (ET/ETR), and digital pre-distortion (DPD) to enable effective spatial multiplexing [10][11]. These strategies strive to ensure linearity and energy efficiency while adapting the various transmission channel constraints [17]-[21][34].

To address these issues, researchers and engineers are experimenting with new approaches to power amplifier design, such as the use of advanced semiconductor technologies like Gallium Nitride (GaN) and Silicon Carbide (SiC), which provides higher power density and improved thermal performance [7][31][33]. Furthermore, cognitive radio-based adaptive approaches and machine learning algorithms are being researched to dynamically modify power amplifier settings depending on changing 5G signal characteristics.

Also, the GaN transistor was employed because of its high prospects with respect to wider bandwidth, higher breakdown voltage, and high thermal dissipation as compared to other transistors which set it as a leading active device for the future designing of RF circuits [9][31]-[32].

In PA design, there is a need to address the satisfaction of a number of criteria in the form of linearity, high-power capability, high efficiency, wide bandwidth as well as high robustness. A tradeoff is also always present in considering the linearity and efficiency during the design of RF power amplifiers [35].

These amplifiers can be classified based on various criteria such as their operating characteristics, circuit configurations, frequency range, and applications. These include Class A Power Amplifiers, Class B Power Amplifiers, Class AB Power Amplifiers, Class C Power Amplifiers, for more envelope varying applications, as well as, Class D Power Amplifiers, Class E Power Amplifiers among others, for more constant envelope applications.

Class A amplifiers run throughout the duration of the input signal. They have the lowest distortion hence the best linearity but are less efficient (usually around 25%) [36]-[41]. Class A amplifiers are widely employed in high-fidelity audio systems and low-power radio frequency (RF) applications that need linearity without care for the efficiency.

Class B amplifiers use just half of the input signal cycle. They are more efficient (up to 78.5%) than Class A amplifiers, although they suffer from crossover distortion at the zero-crossing point [36]-[41]. Class B amplifiers are widely employed in situations where efficiency takes precedence over linearity, such as RF power amplifiers and audio amplifiers for low-power applications.

Class AB power amplifiers tend to inculcate the qualities of both Class A and Class B power amplifiers [10]-[12]. Class C power amplifiers tend to operate for less than half of an input signal cycle. They tend to possess very high efficiencies (usually above 80%) which comes at a cost of severe degradation in linearity. Class C power amplifiers find its use in RF applications that need high efficiency, such as in RF transmitters, RF oscillators, and RF power amplifiers in RF communication systems.

To attain high efficiencies (usually greater than 90%), Class D amplifiers which mainly makes use of pulse-width modulation (PWM) or other switching methods are employed. They have a substantially greater switching frequency than the input signal frequency, necessitating output low-pass filters to eliminate switching harmonics. Class D amplifiers are widely employed in battery-powered devices, audio amplifiers, and high-power applications that need maximum efficiency. Class E, F, and G power amplifiers are specialized power amplifiers that have been optimized for certain applications or needs. Class E amplifiers are very efficient and widely utilized in RF power amplifiers [9].

Class F and Class G amplifiers tend to possess configurations solely intended to increase efficiency without care for the linearity by operating at higher supply voltages or employing strategies that decrease power dissipation [9][32].

Unlike in [23] and [30], our design utilized the GaN HEMT transistor as the active device since it is projected to be the leading active device for RF circuit design [7][31]-[33]. Many forms of matching have been introduced to design PAs as seen in [31] where λ/4 transmission lines (Tlines) equivalent of LC networks [5] coupled with transformers for the matching to optimize the performance of the realized Doherty PA as opposed to single stage hybrid integrated PAs. This PA has increased complexity due to the PA chain (differential and peaking amplifier) with subpar return losses over the band of operation. Also, in [9], a Class AB power amplifier in the L-band of operation is designed using the GaN active device, where the work concentrated on the matching networks being implemented with series stubs and open-ended stubs to act as low pass ladders equivalent in lumped circuits which showed an improved output power and PAE for good PA performance but return losses that were unaccounted for. Then the concept of the determination of the optimum load and source impedances for designing matching networks using load and source pull respectively is introduced in [9][31][33], and to improve the potential of increasing the bandwidth of operation drastically. Then Electromagnetic (EM) simulation as a means of verifying the actual practical PA performance was carried out in [5][9]. In this work, a Class-AB power amplifier utilizing a GaN transistor with an output power of 40.052, PAE of 54.148 %, input return loss of -16.723 dB and output return loss of -20.601 dB, and a small signal gain of 13.634 dB is designed using the Advanced Design System (ADS) software. In the second section, the

methodology that is used for the power amplifier design is explained. In section three, the results obtained from performing various simulations on the realized PA are discussed and the fourth section concludes the whole paper.

2. METHOD (AMPLIFIER DESIGN)

2.1. Selection of Active Device

Many active devices are available for active microwave circuit design but the one utilized for this work was a Gallium Nitride High Electron Mobility Transistor (GaN HEMT) due to its many advantages like its ability to function at high frequencies due to its high electron mobility, as well as providing wider bandwidth, and its ability to operate at high currents since they possess high breakdown voltages which translate to the production of higher output power, among many others. These advantages place it at the forefront as compared to its counterparts in the field of active circuit design. The active device, CGH40010F, obtained from Cree was utilized since it was found from its datasheet [42] to satisfy all the objectives for the proposed power amplifier design. The design objectives stipulated for the proposed power amplifier design is shown in Table 1 below.

Table 1. Design Specifications

Parameter	Specification
Center Frequency	2.4 GHz
Bandwidth	+/- 100 MHz
Output Power	10 Watts (40 dBm)
Gain	> 10 dB
Return Loss	<-12 dB
PAE	>50 %

2.2. DC IV and Bias Point Analysis

The drain and gate bias points were selected based on the information from the datasheet [42]. The device was biased at the quiescent point, and at a gate voltage (V_{GS}) of -2.7 V and a voltage at the drain (V_{DS}) of 28 V, a drain current of 205 mA was produced. These bias points depict the DC operating points for a typical class AB configuration. The simulated I-V characteristics curve for this design is shown in Figure 1 which was very similar to the results in the datasheet for the device.

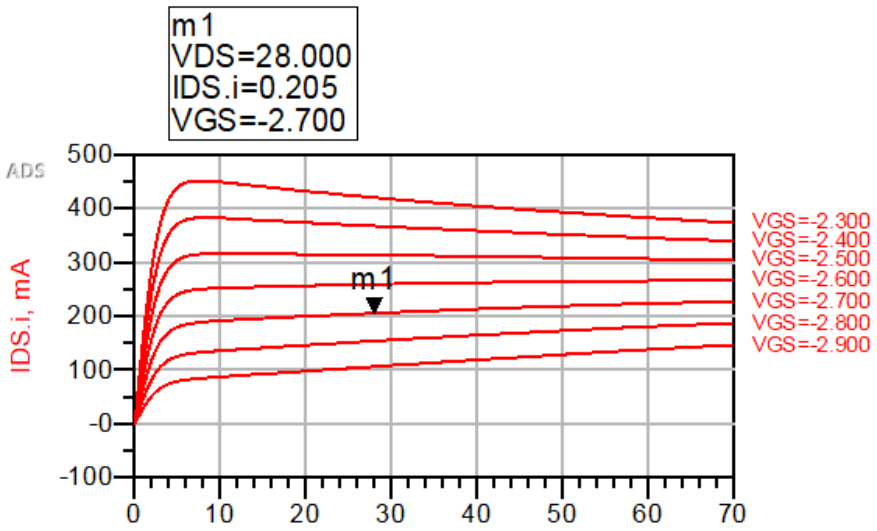


Figure 1. I-V characteristics of GaN HEMT active device

2.3. Stability Analysis

Linearity is one of the main concerns of PA design, as the output is preferred to not deviate from the input signal. This in turn makes the concept of ensuring stability become a major point of note in a power amplifier's design as it is done to prevent the realized PA from behaving like an oscillator rather than a power amplifier due to the presence of a negative resistance on either port of the power amplifier which as it is a typical two-port network.

Also, the power amplifier being a bilateral device, that is a device with both forward and backward transmission, would require a foremost stable design, before the results from the load/source pull can be considered accurate for the matching networks design [32]. This is shown in Equations (1) to (5) [43] which relates the concept where bilateral devices are also stable in nature.
Where;

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1 \quad (1)$$

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \quad (2)$$

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1 \quad (3)$$

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \quad (4)$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 + |\Delta|^2 \quad (5)$$

Since, the power amplifier is a two-port device, its S_{ij} can only have "i" and "j" with a value of either 1 or 2.

In two-port network stability determination, the satisfaction of these equations is vital. They also show how bilateral two-port networks must be stable before accurate impedance matching for gain can be performed on them [43]. It is noted that for $K > 1$ and $B_1 > 0$, or for $K > 1$ and $B_2 > 0$, the two-port device shows unconditional stability, which can also be interpreted as to satisfy the bilateral nature of a two-port device, its stability much be ensured over the frequency band of operation.
The more common metric used on the other hand is the satisfaction of $K > 1$ and $\mu > 1$ (where μ for either source or load from the equations above is determined by interchanging S_{11} and S_{22}) which also shows unconditional stability and is what was used as a metric for determining the stability of the realized power amplifier.

To determine and ensure stability in the designed power amplifier, the utilization of the vector network analyzer in the ADS software was employed, and upon simulation of the resulting circuit, it was shown that the active device was not unconditionally stable over the frequency of interest. Hence, to ensure stability, one of the more utilized methods of ensuring stability in active circuit design was used. This was the implementation of a series resistor connected at the active device's gate (input) terminal.

The choice of which terminal to place the series resistor at the gate of the active was made due to the fact that the resistor is inherently a lossy component and that with respect to power amplifier design, the output terminal is more delicate with respect to the gain. Hence, introducing the series resistor or any lossy components in general at the drain of the active device poses a high risk of causing the total gain obtained from the realized power amplifier to seriously deteriorate and affecting the performance of the active circuit.

The value of the resistance of the series resistor was obtained by manual tuning to be a 5 Ω resistance since at the impedance, the Rollett's factor for stability ($K > 1$) as well as the "mu" condition ($\mu_{source} > 1$ and/or $\mu_{load} > 1$) were completely satisfied resulting in the unconditional stability over the whole spectrum of frequency of operation [43]. In the Figures 2a and 2b, the simulated stability factor as well as the "mu" test of the device are shown respectively and the units shown by the markers are dimensionless in nature.

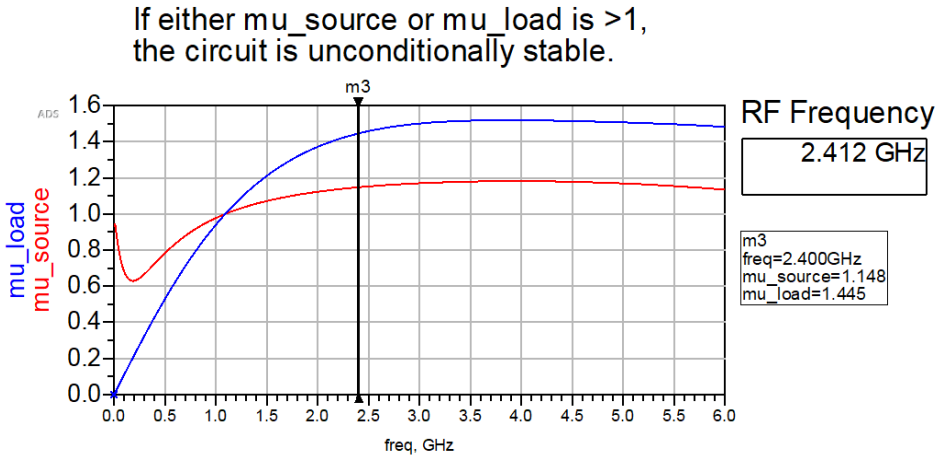


Figure 2a. mu_source and mu _load vs frequency graph

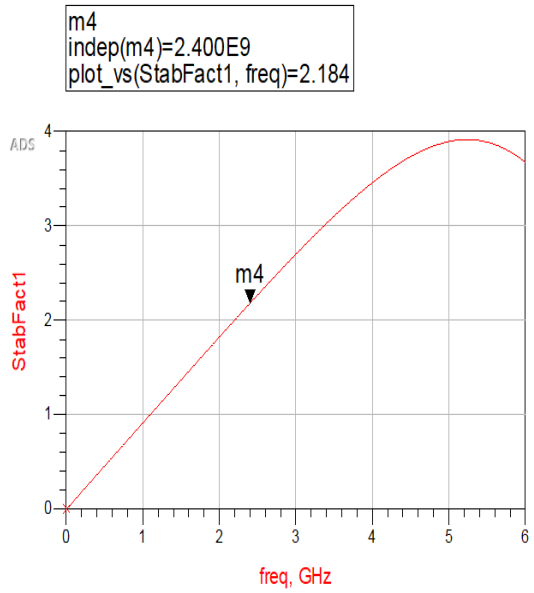


Figure 2b. Graph of stability factor against frequency

2.4. Load-pull Analysis

The next step was to carry out the load-pull and source-pull simulation on the active device. In power amplifier design, these are carried out for the determination of the most suitable impedances for the load and the source respectively, required in the designing of the output and input matching networks. It is basically, finding impedances that provide the best performance for an active microwave circuit in terms of metrics such as maximum output power (P_{out}) as well as maximum PAE over the bandwidth of interest.

To obtain these metrics for the corresponding impedances, those for the source and load are varied respectively in both cases for the source and load-pull analysis.

With respect to this work, the load-pull carried out not only produced the optimum load impedances required for the matching networks, but also its corresponding source impedances hence there was no need to perform a separate source-pull simulation to determine the optimum impedance for the source. This setup consists of a variable source and load impedance, both of which were obtained from the active device's datasheet [42]. These impedances are swept over a range of values in the presence of an RF power input to produce the corresponding achievable output power and PAE values for the active device.

Shown on the Smith Chart in Figure 3 are the load-pull results, which show the power output and PAE contours for an RF input power of 29 dBm. In both the output power circles/contours and that of the PAE, the innermost contours correspond to the highest attainable power output and PAE respectively for the realized power amplifier. Hence, to obtain a resulting class AB operation which has the characteristic of both moderately good

linearity and efficiency, the impedances for matching are chosen as a trade-off between the power output and the PAE and it was found to be "6.414 + 3.880j Ω" for the input impedance and "22.499 - 2.479j Ω" for the output impedance which results in the power at the output of 40.232 dBm and a PAE of 50.57 % at a large signal gain at a value of 11.232 dB.

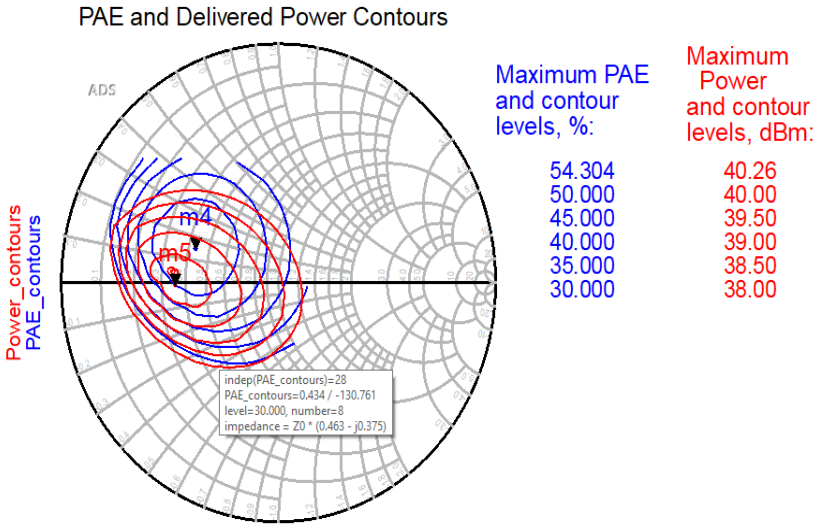


Figure 3. Power and PAE contours in dB and % respectively

2.5. Input and Output Matching Networks Design

The concept of impedance matching in active device design is one of the major considerations in their design process as it directly translates to the amount of power output generated by the power amplifier that will successfully reach the load [32]. It also has a bearing of the efficiency of signal transmission from the input to the output, among many others. The power amplifier is terminated with 50 Ω impedances at both the output and input and these matching networks are responsible for transforming the impedances. At the input side, the 50 Ω termination is transformed to the conjugate impedance of the gate terminal that was obtained from the load pull simulation. At the output side, the impedance of the drain is transformed to that of the 50 Ω termination.

In impedance matching networks, there are many topologies that can be employed based on what is required from the design. It ranges from the most basic L- network match of lumped components, through to T-network matches, π- network matches and then to the more complex distributed cascaded aforementioned matches of transmission lines.

In this work, the output match designed first since the delicacy of the outport terminal with respect to gain was fully taken into consideration. The matching network design was first realized with quarter wavelength ideal transmission lines, with varying characteristic impedances. The choice of transmission lines over lumped components for the matching stemming from the characteristic of transmission lines to operate comparatively better than lumped components in the frequency spectrum of operation (2.3 GHz – 2.5 GHz) that generally tend to exhibit parasitic behavior at these frequencies (above 1 GHz).

This output matching network was based on a topology involving multiple sections of "L" and T-networks which were later optimized to obtain a desirable output match for the conjugate impedance transformation and used a more unconventional approach in the design with the corresponding consideration being discussed. Conversion of the ideal transmission lines into microstrip lines (open and short circuit stubs, as well as series stubs) were then performed. By utilizing the Line Calc feature in ADS, the conversion to microstrip lines was carried out on a Rogers substrate with ϵr = 3.66, 0.7 mm thick, and spaced 25 mil apart. Also, in the network design, three microstrip gaps, represented by the MGAP, along with the parallel capacitors and microstrip lines were employed in the design matching network for the output as is shown in Figure 4.

The capacitors employed in the series part of the network were due to some of the transmission lines originally placed having a large width coupled with a significant length. This made these lines typically function as capacitors in the network due to the inherent characteristic of transmission lines, hence for the practical application of reducing the board size by as much as possible, such a method of replacing them with capacitors altogether was utilized after which optimization was performed to obtain similar operation as their transmission line counterparts.

The open and short circuit stubs were placed in the output matching with the main task of handling the harmonic performance of the realized power amplifier for good gain performance. In the shunt part of the output match, a 50 Ω transmission line was placed which will be in series with the drain voltage source along with the capacitors (acting as RF passes). Its purpose was to carry the large drain current produced by the biasing to the load via the matching network due to the large enough width as well as handle temperature increase in a practical design sense.
Also, the "Tees" and "Steps" were placed between the microstrip transmission line to allow for the mitigation of small reflections from one transmission to another due to the differences in characteristic impedances and also for accurate results in the layout simulation.

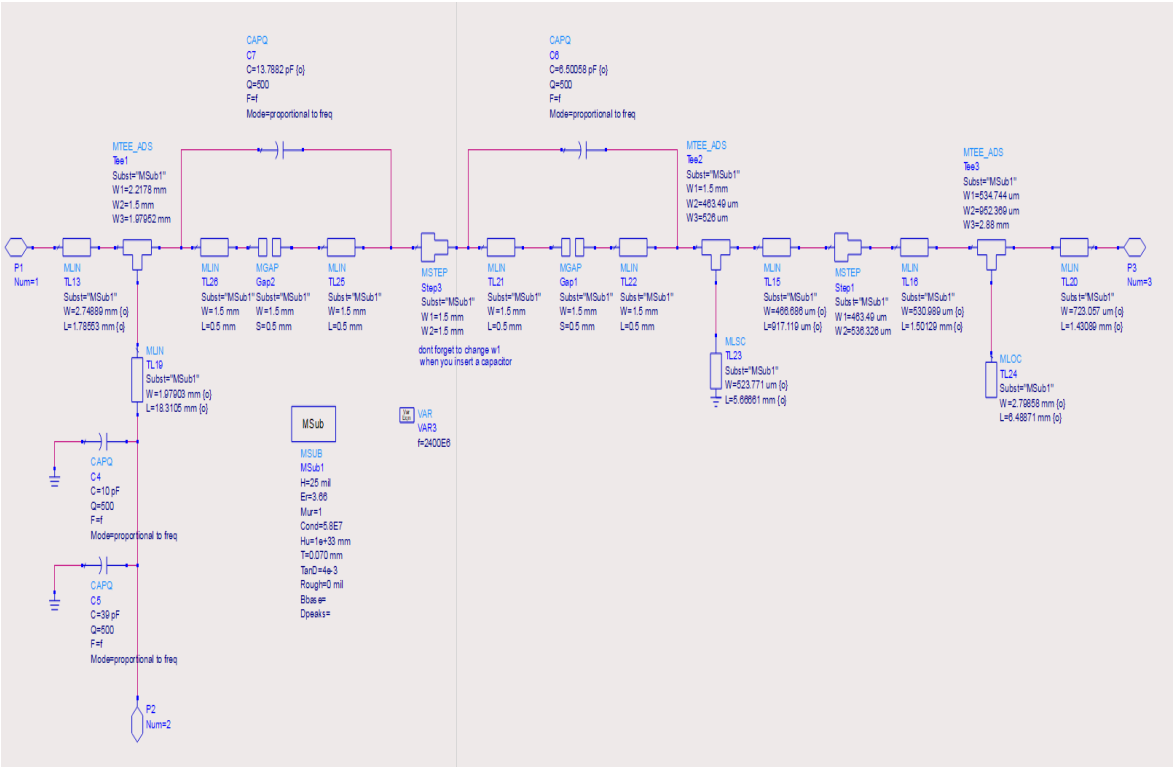


Figure 4. Microstrip output matching network

In designing the matching network for the input, the cascaded L- network topology was employed for matching using a more direct approach, with the Smith chart utility tool. Optimization of the characteristic impedances were then carried out on the ideal transmission lines used to obtain a better match and in Figure 5a, the block diagrammatic setup is shown. The corresponding practical matching network was also done using microstrip lines and a similar process as in the output matching network over the same substrate. With respect to Figure 5b, the matching network at the input for the PA after the conversion from ideal transmission lines to microstrip is shown.

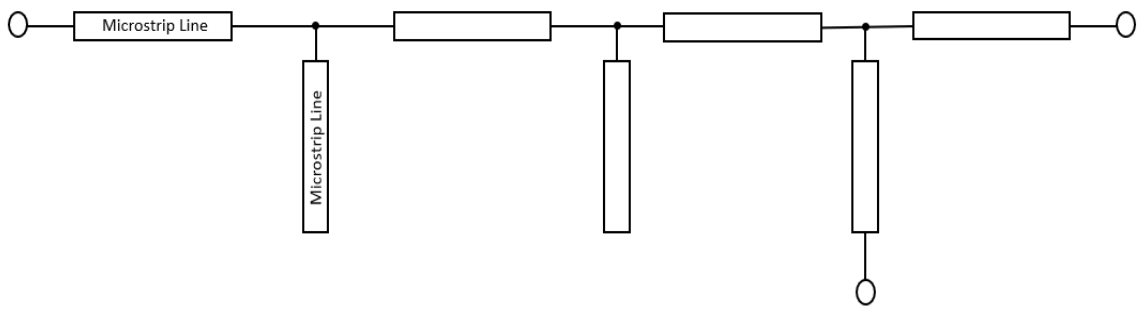


Figure 5a. Block diagram of input matching network

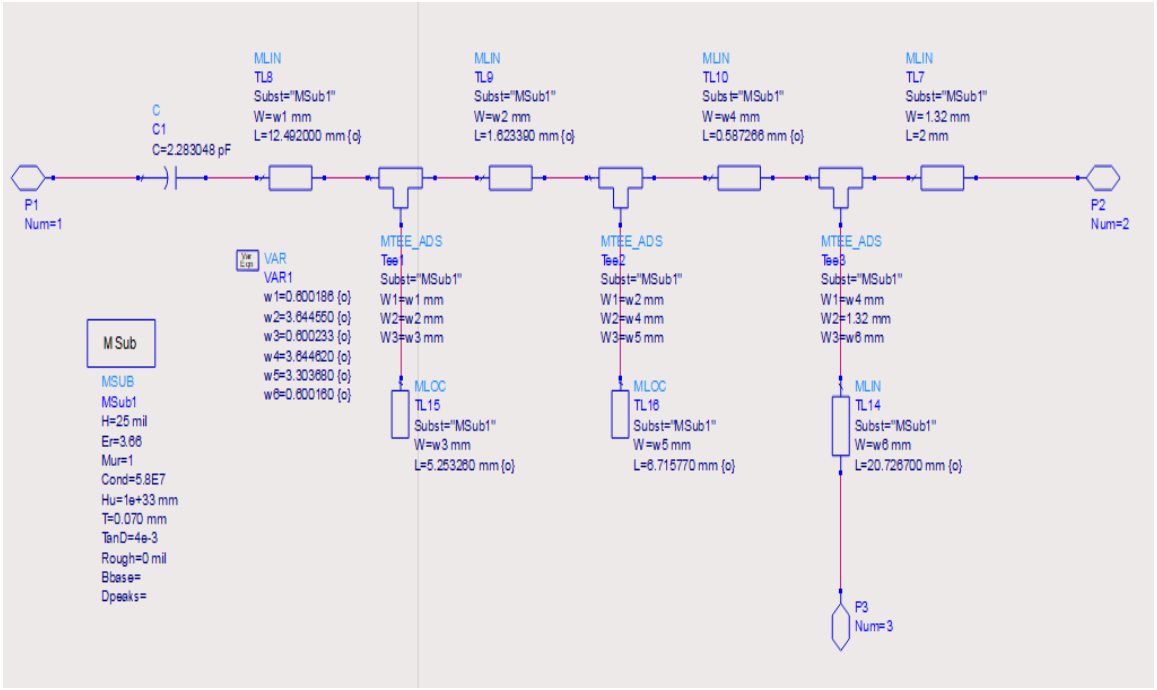


Figure 5b. Practical input matching network

2.4. Amplifier Assembly

This is done to verify the various Figure of Merits (FoMs) for the realized PA design to access performance. At this stage, the various components of the PA have been obtained and the assembly is achieved by integrating these components; the source and load terminations, the matching networks for both the input and output, the bias voltage sources (V_{GS} and V_{DS}), and the active device among many others to obtain the assembled PA schematic as is shown in the Figure 6 below. From the figure, it is also noted that the matching networks were placed in a sub circuit format. The matching network transmission lines for both the input and output match had its values optimized to obtain the desirable goals for the power output, the large signal gain, the return losses, and the small signal gain which were obtained during the load pull simulation stage in the PA design.

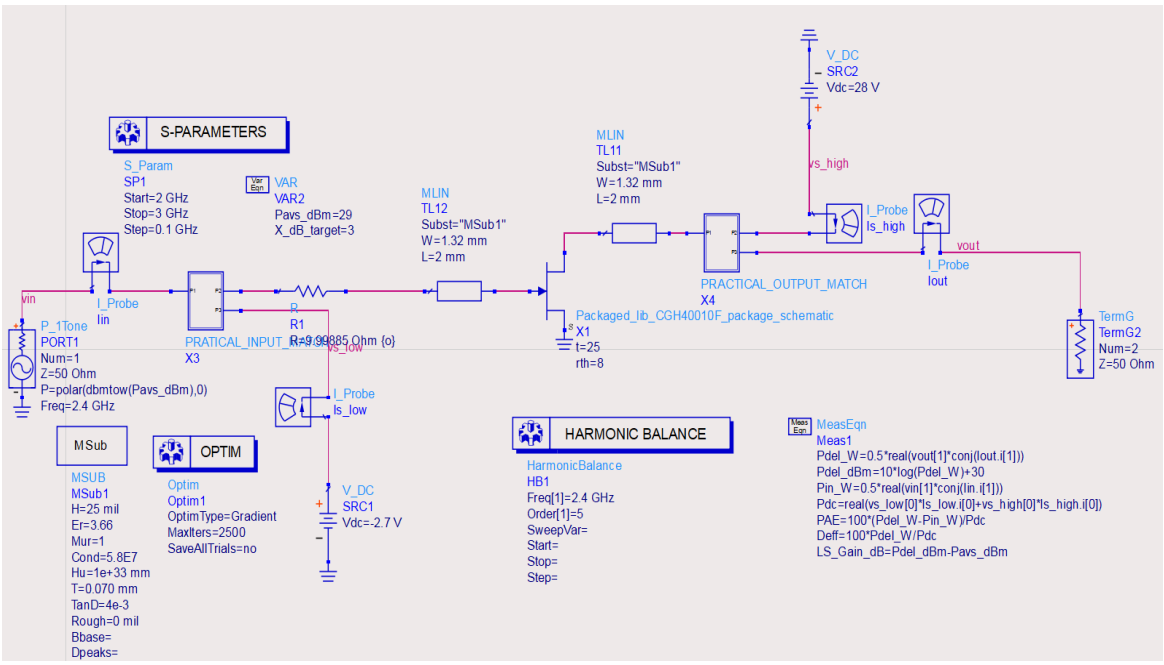


Figure 6. PA Assembly Circuit in schematic view

2.4. Layout Design and Electromagnetic (EM) Co-simulation

Now that the final schematic of the PA had been achieved by assembly of the constituent parts, the practical implementation of the PA circuit is realized and tested for satisfiability with the design goals set for the PA in the earlier section. Both were performed to determine the proposed power amplifier's performance in the real world upon its actual fabrication with real world effects at play. EM Momentum simulation was then run on the generated layout over the frequency band of operation of the active device, i.e. 1 GHz – 6 GHz, after which a layout symbol was generated to similar to the layout view. This layout was then implemented in tandem with the corresponding schematic power amplifier components that could not be obtained from the layout design due to their lack of the layout footprint. This was for validating the realized power amplifier's performance through co-simulation of the layout part of the design with the schematic part. Figure 7 shows the layout of the proposed PA for EM co-simulation verification. This shows the representation of a potential PA design when it is fabricated using transmission lines over a PCB board. It is noted that this design is still in its simulation stage and has not been fabricated yet.

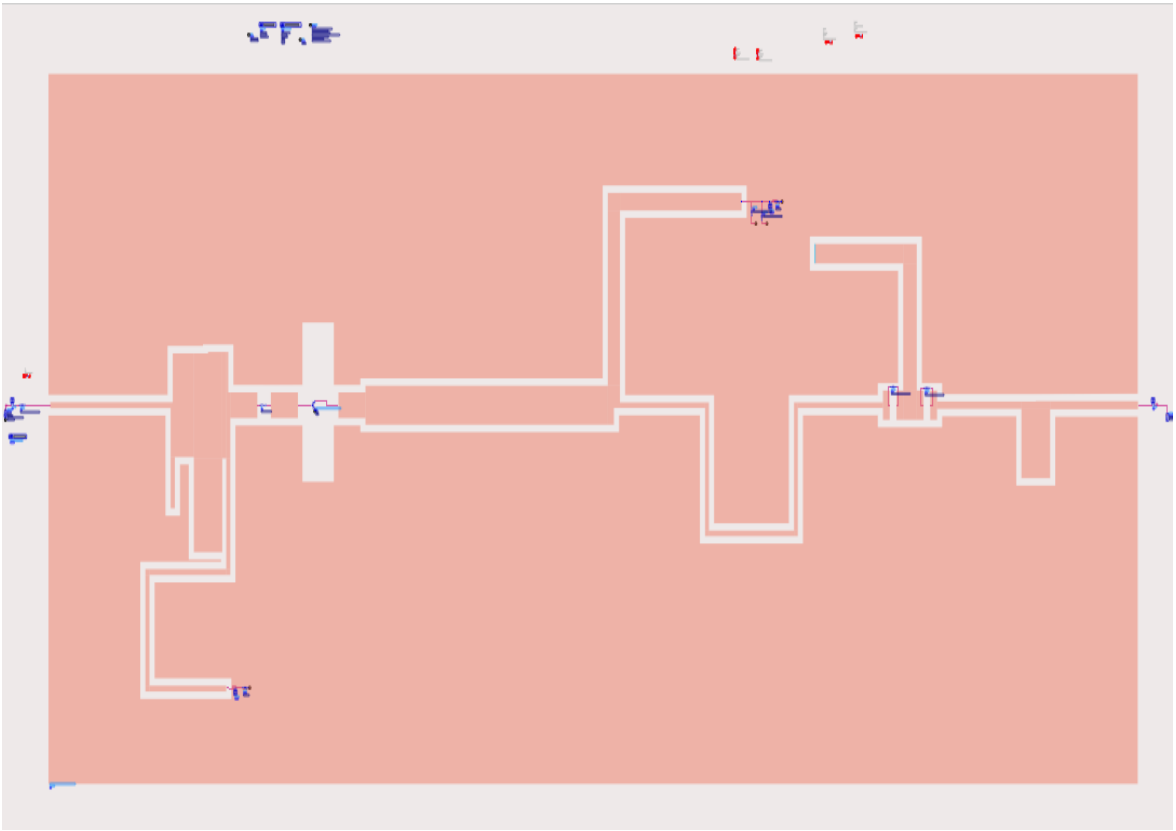


Figure 7. PA Layout Design

3. RESULTS AND DISCUSSION

Upon obtaining the complete PA schematic and its corresponding layout view, various simulations to validate the performance of the PA were executed at the chosen bias points (I_{DS} = 205 mA, V_{GS} = -2.7 V, V_{DS} = 28 V) for operation in the Class AB region. Both large signal and small signal simulation measurements were carried out to validate the power amplifier's performance. In Figure 8a, the voltage and drain current waveforms obtained at the power input of 29 dBm are shown. As is observed, the power amplifier exhibits a linear operation due to the sinusoidal nature of the drain voltage's waveform at the input power (with 5 W high efficiency). Also, the waveforms of the drain current show a mode of operation in the Class AB region for the power amplifier since the current conduction angle as shown in the Figure 8a is typically more than 180° but less than the completion of a full cycle of 360°, a major characteristic of class AB configuration power amplifiers.

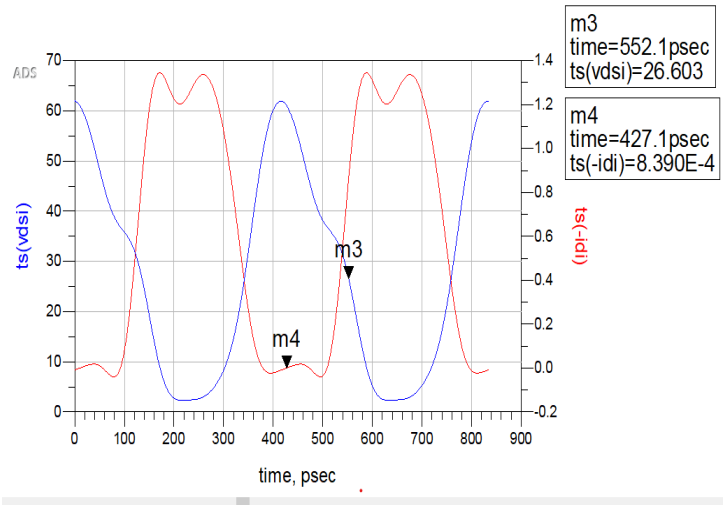


Figure 8a. Waveforms of the drain current and voltage

S-parameter characteristics, i.e. the small signal results of the realized power amplifier are shown below in the Figures 8b and 8c and they tend to satisfy all the design objectives of the designed PA over the frequency of 2.3 GHz - 2.5 GHz.

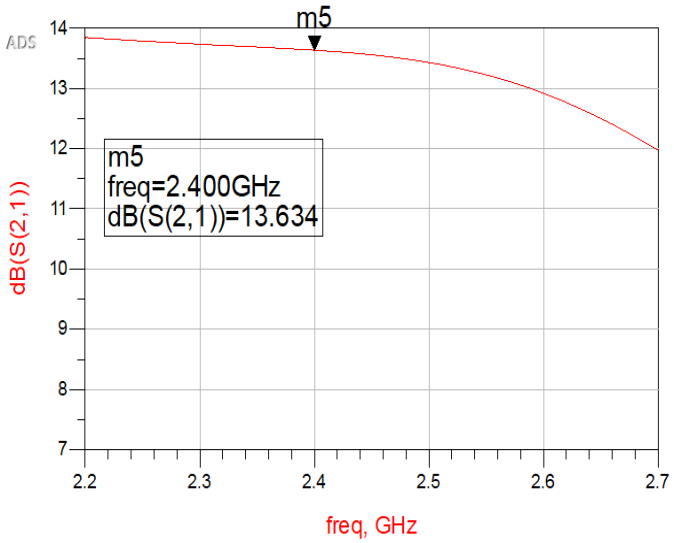


Figure 8b. Graph of small signal gain over the frequency band

Figure 8b above shows the small signal gain (S_{21}) of the power amplifier depicting the power output's ratio to the input power in simple terms. It shows a value above 12 dB over the bandwidth of operation for the proposed PA after EM co-simulation was performed which is very desirable since generally the figure of merits for any active design tend to deteriorate especially after it is realized in its layout mainly due to the "parasitics" acting the design due to real world effects.

The strength of the reflected signal caused by the discontinuous nature existing between transmission lines other components in the PA design was measured which in the domain of RF and microwave engineering is generally termed as return loss. This is any form of discontinuity that is present the termination of a transmission line and its characteristic impedance and is very important in the realm of power amplifier design since it can severely impart the strength of the output signal's power. In Figure 8c, the return losses at the input and output of the realized power amplifier were depicted after EM co-simulation was performed as was done to obtain all the other results showcased in this section of the work.

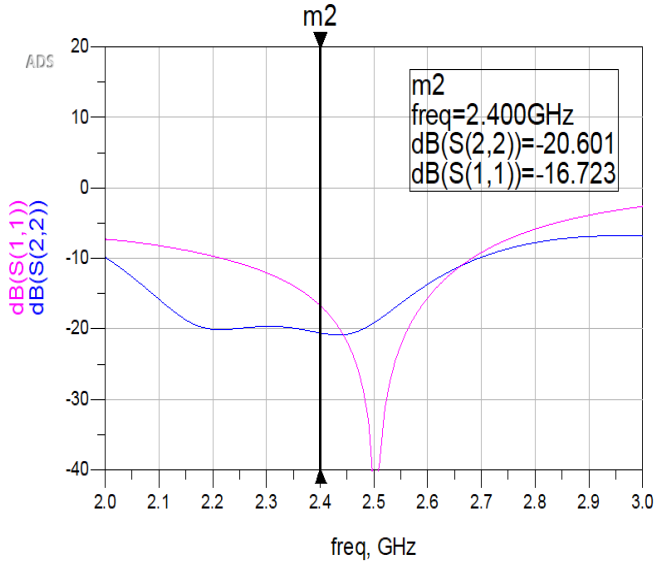


Figure 8c. Graph of return losses at the input and output of the realized PA

It is noted from the Figure 8c that the return losses at both the input and output are lesser than -12 dB over the bandwidth of operation with values of -16.726 dB and -20.601 dB respectively at the center frequency of the PA. This shows very good matching as in active design, the threshold return loss value is -10 dB.
It also satisfies the goals for the realized power amplifier design and this can be attributed to the setup used in designing our output matching network to ensure robustness and the later optimization of the entire matching networks that was performed after the schematic PA assembly even after performing EM co-simulation.

3.1. One-Tone Simulation

Here, the PA is simulated from dc, a fundamental frequency (the center frequency) and its corresponding integer multiples. This was for the determination of the corresponding interferences from these other frequencies in the form of spurious signals introduced during the processing of an input signal for its amplification as compared to the power amplifier's actual output power. The harmonic spectrum representation of the power output is 40.052 dBm at the frequency of operation of 2.4 GHz for a 29 dBm input power and negligible power output at these other "integer multiple" frequencies as is shown in Figure 9a.

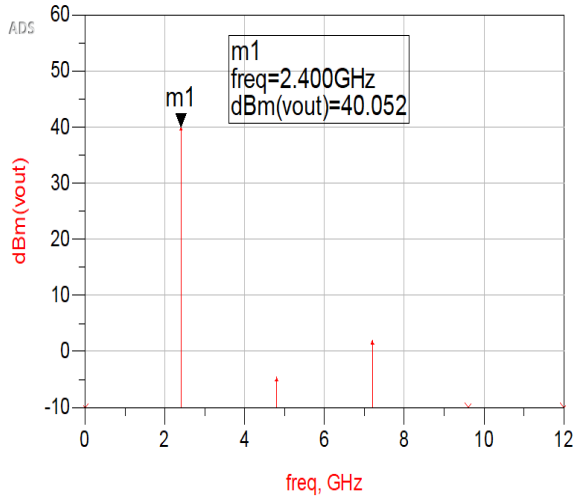


Figure 9a. Output power harmonic spectrum representation

To complete the performance evaluation of the PA in terms of the Figure of Merits, the PAE and drain efficiency of the realized PA were found. The drain efficiency depicts the RF power output's ratio to that of the DC input of the PA. The PAE however factors in the contribution of the RF input power along with the DC input that produced a certain output. This makes it a more desirable Figure of Merit to determine the efficiency of a given PA. Figure 9b below shows the drain efficiency as well as PAE at the input power of 29 dBm and it is seen that the PAE shows a PAE of around 55 % which is around the typical PAE for Class AB Configuration operation also attained from the optimization of the matching networks.

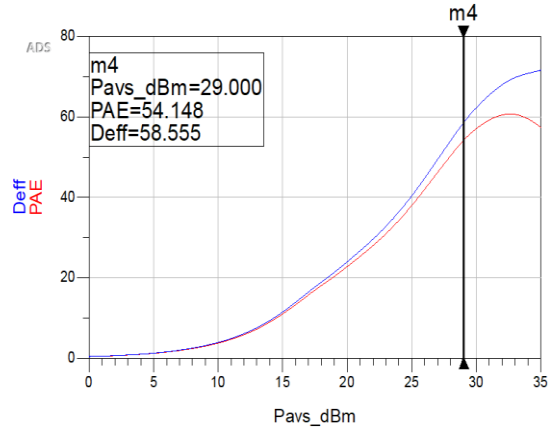


Figure 9b. PAE & Drain efficiency vs power input.

Now, the concept of compression where an output power reduces by an 'X' dB value was addressed in our PA verification. The 3 dB compression point was of concern in the realized as it is the most common characterization of compression analysis in power amplifier design. This gain compression point for the realized PA is found to be around 10.236 dB at a corresponding input power of 30.600 dBm as is shown in the Figure 9c below. It is found from the relation between the input power and output power and is shown in the Equations (6) and (7) below where P_{in} represents the input power and P_{out} represents the power at the PA's output.

$$P_{in}(\text{dBm}) = P_{\text{out}}(\text{dBm}) - (\text{3dB compression gain}) \tag{6}$$

$$\text{3dB compression gain} = \text{linear gain} - \text{3 dB} \tag{7}$$

The idea is for the input power that causes a corresponding 3 dB compression to be greater than the actual input power used to excite the power amplifier hence preventing such a compression. Figure 9d shows that the 3 dB compression for the proposed PA occurs at 30.6 dBm input power which is greater than the RF input signal power used to excite the realized power amplifier (P_{in} = 29 dBm) which satisfies the metric for power amplifier compression analysis hence showing good performance in terms of compression.

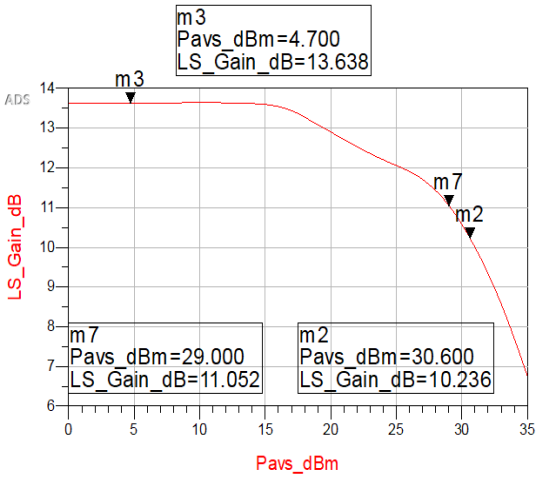


Figure 9c. Large signal gain vs. input power

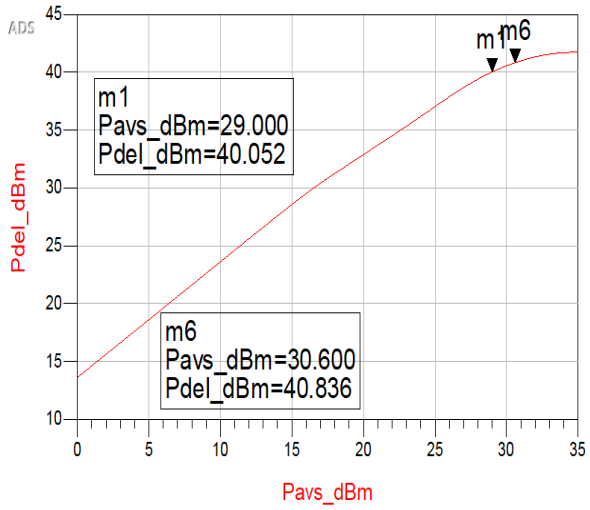


Figure 9d. Output power vs. input power of realized PA.

3.2. Two-Tone Simulation

Here, two signals of small frequency variation were passed through the power amplifier to determine the level of nonlinearity in a PA when comparing spurious signal components that cannot be filtered out at the output due to their close proximity to the power amplifier's center frequency of operation.

The intermodulation products of the third order (IMD3), which were determined for the power amplifier, are of major concern in characterizing a power amplifier since the higher orders are further from the center frequency and hence possess a higher likelihood of being filtered out.

For the two-tone analysis in this design, an offset frequency of 1 MHz from the center frequency of 2.4 GHz for the power amplifier design, for intermodulation distortion at the input signal power of 29 dBm was utilized.

Intermodulation Distortion Suppression Value, which was determined for the level of distortion in the design, is deined as the difference between signal level of the fundamental signal and that of the 3rd harmonic components [8]. In this work, these signal levels were obtained from frequencies; 2.401/2.399 GHz and 2.397/3.403 GHz for the first order and the third order components respectively, with the focus on the signal value of third order frequency. Figure 10 below shows the two-tone behavior of the proposed PA after performing EM co-simulation.

The IMD suppression value was determined from the Equation (8) below:

$$32.212 - 4.331 = 27.881 \text{ dBc} \tag{8}$$

This value shows the large difference in signal output existing between the fundamental frequency and the third order product. This shows that the signal distortion poses minimal effects when compared to the fundamental signal, which is the desirable signal for the design operation.

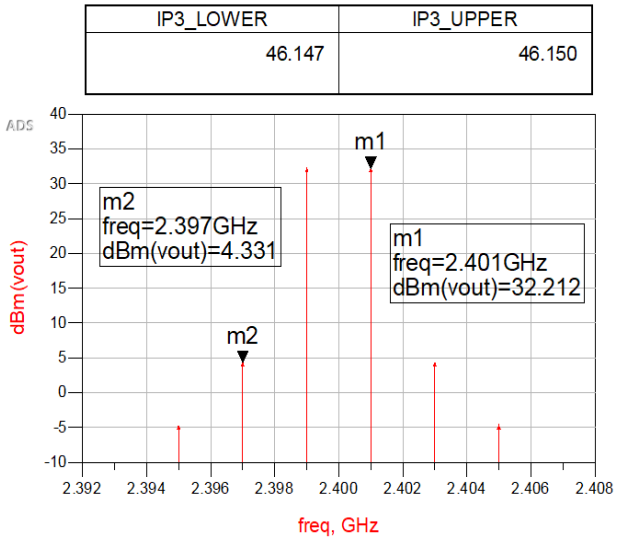


Figure 10. Third-order intermodulation products of the proposed PA

From the Figure 10, the IP3_LOWER and IP3_UPPER values represent third-order intercept point (in dBm) at the output of the power amplifier [8]. Also, the offsets for the frequency of operation at 2.4 GHz have their third order intermodulation products measurements shown, where the obtained third order intercept point for the upper frequency (OIP3 Upper) was 46.150 dBm and for the lower frequency (OIP3 Lower) was 46.147 dBm. This also shows good performance of the power amplifier designed since the values obtained are considerably more than the actual output power (10 W). This is because these measurements represent the maximum power outputs that can be processed by the realized PA before third order intermodulation distortion sets in to cause non-linearity in the designed power amplifier.
Below is Table 2 which depicts the performance of the proposed design in comparison to other reported designs.

Table 2. PA Performance Comparison

Ref.	[7]	[9]	[23]	[33]	This Work
Frequency (GHz)	0.4	1.6	0.9	2	2.4
Bandwidth (GHz)		0.4	1	0.5	0.2
Type	Class AB	Class AB		Class AB	Class AB
Small Signal gain (dB)	27.8	-	-	-	13.634
Large signal gain (dB)		11~14	14.83	12	~11 dB
P_o(dBm)	24.2	39~41.05	43.5	>40	40.052
PAE (%)	43.8	43.6 ~ 55.4	60	>47	54.148
Input Return Loss (dB)	-	-	-	-	<12 dB
Output Return Loss (dB)	-	-	-	-	< 12dB
Complexity	Two- stage PA	Single stage PA	Parallel PA combination (Doherty)	Single stage PA	Single stage PA
Technology	30nm CMOS	GaN	MOSFET	GaN	GaN

4. CONCLUSION AND RECOMMENDATIONS

The design process for a 10W wideband power amplifier utilizing the GaN HEMT technology at 2.4 GHz was presented in this work. A load-pull simulation was used for the determination of the ideal impedances at the source and load needed to achieve the highest output power (Pout) and highest PAE over the targeted bandwidth of 200 MHz. Optimization was then done on the matching networks upon PA assembly to provide good matching, power output and PAE response. Measurements of both small and large signals are made to evaluate the effectiveness of the amplifier in both linear and non-linear operations respectively.

The linear gain for the proposed power amplifier is 13.634 dB at 2.4 GHz. The measured output power for an input power of 29 dBm is 40.052 dBm, and its corresponding PAE is 54.148% with both input and output return losses below -12 dB over the bandwidth of operation (2.3-2.5 GHz).
The PAE for the proposed PA can however be increased by making that the main goal of the optimization in the matching networks but it comes at the cost of the severe degradation of the return loss. Also, the use of the

resistor being a lossy device for the stability of the PA limited both the dc operating capabilities of the PA as well as the gain. A more elaborate stability matching network design through an iterative process would likely address such a case.

REFERENCES

[1] I. S. Akila, S. M. Logesh Raj, R. Adhavan and K. S. Vignesh, "Design of GaN HEMT Class AB Amplifier at 4.48 GHz for 5G Connectivity," in *2024 International Conference on Inventive Computation Technologies (ICICT)*, Lalitpur, Nepal, 2024. https://doi.org/10.1109/ICICT60155.2024.10544570

[2] A. Ahsan, S. Sutradhar and M. J. Akhtar, "Design of Wideband Class AB Power Amplifier Using Improved SRFT Matching for Low Power Applications," in *2024 IEEE Asia-Pacific Microwave Conference (APMC),*, Bali, Indonesia, 2024.

[3] S. Ozan, A. Pitt, M. Nair, M. A. Beach and T. Cappello, "A 47 % Fractional Bandwidth Sequential Power Amplifier with High Back-off Efficiency," in *2022 4th IEEE Middle East and North Africa COMMunications Conference (MENACOMM), Amman, Jordan*, 2022. https://doi.org/10.1109/MENACOMM57252.2022.9998195

[4] X. Li, D. Cheng, X. Jiang, D. Wang and L. Li, "A 57-71-GHz Accurate dB-Linear Variable Gain Power Amplifier with Ultralow Gain Error Using Particle Swarm Optimization Algorithm," in *International Microwave Symposium - IMS 2024*, Washington, DC, 2024. https://doi.org/10.1109/IMS40175.2024.10600450

[5] H. Zahid, M. K. Saleem and A. Maalik, "A High Efficiency 25W Class-AB and Class-F GaN High Power Amplifier at 10 GHz for Satellite Applications," in *2023 25th International Multitopic Conference (INMIC), Lahore, Pakistan*, 2023. https://doi.org/10.1109/INMIC60434.2023.10466191

[6] S. Bae, J. Jeon, S. Hwang, B. Yoon and J. Kim, "A Highly Linear and Efficient Differential Power Amplifier with 35-dBm Saturated Output Power, 65% Peak PAE by Reducing Base Voltage Peaking in InGaP/GaAs HBT Process for Handset Applications," in *2024 IEEE/MTT-S International Microwave Symposium - IMS 2024*, Washington, DC, USA, 2024. https://doi.org/10.1109/IMS40175.2024.10600329

[7] H. Gao, X. Wu, Y. Yang, K. Huang, X. Yu and Y. Li, "A High Linearity Class AB Power Amplifier for Sub-1 GHz Applications," in *2022 IEEE MTT-S International Wireless Symposium (IWS)*, Harbin, China, 2022. http://dx.doi.org/10.1109/IWS55252.2022.9977944

[8] C. Majumder, B. Majumder and B. Ghosh, "A kW-range Solid-State Power Amplifier Design for OTH Radar's Transmitter Application," in *2023 IEEE Microwaves, Antennas, and Propagation Conference (MAPCON)*, Ahmedabad, India, 2023. http://dx.doi.org/10.1109/MAPCON58678.2023.10463952

[9] M. Chegini, H. Nemati and M. Kamarei, "A New 10 Watt 1.6 GHz Linear Power Amplifier with More Than 11 dB Gain," in *2023 31st International Conference on Electrical Engineering (ICEE)*, Tehran, Iran, Islamic Republic of, 2023. https://doi.org/10.1109/ICEE59167.2023.10334785

[10] Z. Ma and S. Mohammadi, "A Reliable 5G Stacked Power Amplifier in 45nm CMOS Technology," in *2023 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications*, Las Vegas, NV, USA, 2023. https://doi.org/10.1109/PAWR56957.2023.10046289

[11] K. S. Prasad, P. Hemanth and D. Mandal, "A Rail-to-Rail Input Class-AB Linear Amplifier with Improved Bandwidth and Slew-Rate for Envelope Tracking Supply Modulators," in *2024 IEEE International Symposium on Circuits and Systems (ISCAS)*, Singapore, Singapore, 2024. https://doi.org/10.1109/ISCAS58744.2024.10558486

[12] I. Peppas et al., "A 3.6GHz Highly Efficient Dual-Driver Doherty Power Amplifier," in *2024 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*, San Antonio, TX, USA, 2024. https://doi.org/10.1109/PAWR59907.2024.10438577

[13] Z. Zhang, A. Piacibello and V. Camarchia, "Efficiency versus linearity trade-off in an S-band class-AB power amplifier," in *2023 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications*, Las Vegas, NV, USA, 2023. https://doi.org/10.1109/PAWR56957.2023.10046214

[14] M. S. Mugisho, C. Friesicke, M. Ayad, T. Maier and R. Quay, "Harmonic-Injection Doherty Power Amplifier: Benefits and Limitations," in *2024 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*, San Antonio, TX, USA, 2024. https://doi.org/10.1109/PAWR59907.2024.10438621

[15] B. Cimbili, C. Friesicke, F. Van Raay, S. Wagner, M. Bao and R. Quay, "High-Efficiency Watt-Level E-band GaN Power Amplifier with a Compact Low-loss Combiner," in *2023 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications*, Las Vegas, NV, USA, 2023. https://doi.org/10.1109/PAWR56957.2023.10046243

[16] N. Utomo et al., "An 85.1% Peak Efficiency, Low Power Class H Audio Amplifier With Full Class H Operation," *IEEE Transactions on Circuits and Systems I: Regular Papers,* pp. 4692-4704, Dec 2023. https://doi.org/10.1109/TCSI.2023.3305622

[17] L. Letailleur, M. Villegas, A. Al Hajjar and C. E. Kacou, "Characterization of GaN Power Amplifier Using 5G mm-Wave Modulated Signals," in *2023 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications*, Las Vegas, NV, USA, 2023. https://doi.org/10.1109/PAWR56957.2023.10046272

[18] D. V. Kleimenkin, M. A. Sergeenko, A. A. Zhuk, N. N. Prokopenko, "Class AB Differential Stage on Complementary Field-Effect Transistors (CJFET, CCMOS) and Inclusion Schemes in Micro-Power High-Speed Operational

Amplifiers," in *024 Wave Electronics and its Application in Information and Telecommunication Systems (WECONF)*, 2024. http://dx.doi.org/10.1109/WECONF61770.2024.10564615

[19] A. Afifi, H. Ragaai and M. El-Nozahi, "Class AB Power Amplifier with A Differential Cold-FET Pre-Distorter," in *2024 13th International Conference on Communications, Circuits and Systems (ICCCAS)*, Xiamen, China, 2024. http://dx.doi.org/10.1109/ICCCAS62034.2024.10652774

[20] M. Zhang, X. Wang, H. Liu, X. Qi, X. Li and S. Wang, "Class-AB Operational Amplifier with Current Domain Slew-Rate Enhancement," in *2022 IEEE 5th International Conference on Electronics Technology (ICET)*, Chengdu, China, 2022. https://doi.org/10.1109/ICET55676.2022.9824805

[21] H. Miao, "Design and Performance Analysis of a Frequency Modulation (FM) Transmitter: Integrating Voltage Controlled Oscillator and Class AB Power Amplifier," in *2024 IEEE 6th International Conference on Civil Aviation Safety and Information Technology (ICCASIT)*, 2024.

[22] B. Cimbili, C. Friesicke, S. Wagner, M. S. Mugisho, M. Bao and R. Quay, "Investigating Feeding Techniques for High-power and High-efficiency E-band Power Amplifiers," in *2024 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*, San Antonio, TX, USA, 2024. https://doi.org/10.1109/PAWR59907.2024.10438614

[23] V. Seldyukova and E. Balashov, "20 W 900 MHz Doherty Power Amplifier," in *2022 International Conference on Electrical Engineering and Photonics (EExPolytech)*, St. Petersburg, Russian Federation, 2022. http://dx.doi.org/10.1109/EExPolytech56308.2022.9950977

[24] M. Schutz, J. -D. Bertaux and L. Bacqué, "Accurate Measurement and Control Sytem for RF Broadband Power Amplifier," in *2023 IEEE Symposium on Electromagnetic Compatibility & Signal/Power Integrity (EMC+SIPI)*, Grand Rapids, MI, USA, 2023. https://doi.org/10.1109/EMCSIPI50001.2023.10241584

[25] Z. Chen et al., "A 26-GHz Linear Power Amplifier with 20.8-dBm OP1dB Supporting 256-QAM Wideband 5G NR OFDM for 5G Base Station Equipment," in *2023 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, San Diego, CA, USA, 2023. https://doi.org/10.1109/RFIC54547.2023.10186174

[26] P. S. Niklaus, J. W. Kolar and D. Bortis, "100 kHz Large-Signal Bandwidth GaN-Based 10 kVA Class-D Power Amplifier With 4.8 MHz Switching Frequency," *IEEE Transactions on Power Electronics,* vol. 38, no. 2, pp. 2307-2326, 2023. https://doi.org/10.1109/TPEL.2022.3213930

[27] J. Gu et al., "A 23-30 GHz 4-Path Series-Parallel-Combined Class-AB Power Amplifier with 23 dBm Psat, 38.5% Peak PAE and 1.3° AM-PM Distortion in 40nm Bulk CMOS," in *2023 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, San Diego, CA, USA, 2023. https://doi.org/10.1109/RFIC54547.2023.10186197

[28] S. A. Zainol Murad, A. F. Hasan and F. A. Bakar, "Design of 3.5 GHz Cascode CMOS Class E Power Amplifier for 5G Application," in *2024 IEEE 1st International Conference on Communication Engineering and Emerging Technologies (ICoCET)*, Kepala Batas, Penang, 2024. https://doi.org/10.1109/ICoCET63343.2024.10730124

[29] Fazel Ziraksaz, Alireza Hassanzadeh, "Design of a High-Efficiency Deep Bias Class-AB Power Amplifier With 70% PAE at P 1dB," in *2023 5th Iranian International Conference on Microelectronics (IICM)*, 2023. https://doi.org/10.1109/IICM60532.2023.10443139

[30] H. Shihai, J. Liang, X. Linjian, H. Meng and Y. Qian, "A High Efficiency and High Linearity GaAs HBT Doherty Power Amplifier for 5G NR 3.4V Application," in *IEEE/MTT-S International Microwave Symposium - IMS 2024*, Washington, DC, USA, 2024. https://doi.org/10.1109/IMS40175.2024.10600295

[31] E. N. Mohamed, A. M. Elelimy Abounemra, M. Darwish and A. M. El-Tager, "A Highly Linear and Efficient GaN RF Power Amplifier for Telemetry Applications in S-Band," in *2024 International Microwave and Antenna Symposium (IMAS)*, Marrakech, Morocco, 2024. https://doi.org/10.1109/IMAS61316.2024.10818190

[32] A. Piacibello, J. J. Moreno Rubio, R. Quaglia and V. Camarchia, "AM/PM Characterization of Wideband Power Amplifiers," in *2022 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*, Las Vegas, NV, USA, 2022. https://doi.org/10.1109/PAWR53092.2022.9719787

[33] M. Chegini, M. Kamarei and H. Nemati, "A New Design for 1.75 to 2.55 GHz GaN Power Amplifier with More Than 40 dBm Output Power and 12 dB Maximum Gain," in *A New Design for 1.75 to 2.55 GHz GaN Power Amplifier with More Than 40 dBm Output Power and 12 dB Maximum Gain," 2023 5th Iranian International Conference on Microelectronics (IICM)*, Tehran, Iran, Islamic Republic of, 2023. https://doi.org/10.1109/IICM60532.2023.10443204

[34] D. Y. C. Lie, J. C. Mayeda, C. Sweeney, G. Somasundaram and J. Lopez, "Broadband Linear and Highly-Efficient Millimeter-Wave Power Amplifiers Design in 5G FR2 Band," in *2023 Asia-Pacific Microwave Conference (APMC*, Taipei, Taiwan,, 2023. https://doi.org/10.1109/APMC57107.2023.10439702

[35] H. Ordouei and F. Gerfers, "Energy-efficient D-Band Power Amplifier Linearization Adopting Back-Gate Feedforward Technique in 22nm FD-SOI," in *2024 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*, San Antonio, TX, USA, 2024. https://doi.org/10.1109/PAWR59907.2024.10438580

[36] Komlosi Bogdan-Flavius, Bonciog Dumitru-Daniel, Maranescu Valentin-Ioan, "Enhancing Audio Performance: Noise Reduction and Efficiency in Class AB Amplifier Design," in *2024 International Symposium on Electronics and Telecommunications (ISETC)*, 2024. http://dx.doi.org/10.1109/ISETC63109.2024.10797394

[37] H. Zheng, X. Li and W. Xiao, "Super Class AB Buffer Amplifier with ICMR and Gain Enhancement for LED Backlight Driver," in *2023 6th International Conference on Electronics Technology (ICET)*, Chengdu, China, 2023. https://doi.org/10.1109/ICET58434.2023.10211643

[38] S. F. Gorgadze and A. A. Maksimov, "Technique for Studying Mobile Communications Systems Signal Power Amplifier Efficiency," in *2022 Systems of Signals Generating and Processing in the Field of on Board Communications*, Moscow, Russian Federation, 2022. https://doi.org/10.1109/IEEECONF53456.2022.9744400

[39] J. Böhler et al., "Ultra-High-Bandwidth Power Amplifiers: A Technology Overview and Future Prospects," *IEEE Access,* vol. 10, pp. 54613-54633, 2022. https://doi.org/10.1109/ACCESS.2022.3172291

[40] T. Lecocq, E. Kerhervé and J. -M. Pham, "NB-IoT High Linear Doherty Amplifier with Active Balun," in *2022 20th IEEE Interregional NEWCAS Conference (NEWCAS)*, Quebec City, QC, Canada, 2022. https://doi.org/10.1109/NEWCAS52662.2022.9842261

[41] J. Ma, M. Nair, G. Watkins, K. Morris and M. Beach, "Linearity Optimisation for Multi-Bit Digital Power Amplifier," in *2022 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR)*, Las Vegas, NV, USA, 2022. https://doi.org/10.1109/PAWR53092.2022.9719716

[42] Wolfspeed, "CGH40010F Data Sheet," [Online]. Available: https://www.aipcba.com/datasheet/pdf/cgh40010f-cm98480892-f75986281.html?page=1.

[43] D. M. Pozar, Microwave Engineering, vol. IV, John Wiley & Sons, Inc, 2012, pp. 564-570.

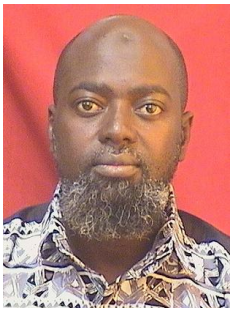
[44] D. V. Kleimenkin, M. A. Sergeenko, A. A. Zhuk, N. N. Prokopenko, "Class AB Differential Stage on Complementary Field-Effect Transistors (CJFET, CCMOS) and Inclusion Schemes in Micro-Power High-Speed Operational Amplifiers," in *2024 Wave Electronics and its Application in Information and Telecommunication Systems (WECONF)*, 2024. http://dx.doi.org/10.1109/WECONF61770.2024.10564615

BIOGRAPHIES OF AUTHORS

Joshua Aa-Daaryeb Nounyah obtained his Bachelor of Science degree in Telecommunication Engineering from Kwame Nkrumah University of Science and Technology in 2022. He has since dedicated himself to research in the field of Rf/microwave circuit design where he took a role as a research assistant with the Department of Telecommunication Engineering at his alma mater.

Bernice Pormaa Ansu is currently pursuing an MPhil in Telecommunication Engineering at Kwame Nkrumah University of Science and Technology, where she previously completed her undergraduate degree. Her study focuses on the convergence of cybersecurity, communication, and networking.

Mensah Emmanuel pursued a BSc in Telecommunication Engineering, a 4-year degree program at Kwame Nkrumah University of Science and Technology. He's currently learning basic machine learning modules and frameworks using the Python Programming Language.



Abdul-Rahman Ahmed has been a lecturer in the Department of Electrical and Electronic Engineering since December 2005. He received his BSc. Degree in Electrical/Electronic Engineering from the Kwame Nkrumah University of Science and Technology in 2002 and was retained by the department to serve as a teaching assistant until 2003 when he received a British Government Scholarship to undertake a postgraduate program in Radio Systems Engineering at the University of Hull, U.K. He returned in 2005 to join the Department of Electrical and Electronic Engineering and subsequently went further to obtain a PhD in Radio Sciences and Engineering from Chungnam National University in South Korea in 2014. He has been teaching mainly telecommunication courses to undergraduate and postgraduate students in the Telecommunication Engineering program of the faculty.
His teaching includes courses in Electromagnetic Fields Theory, Electromagnetic Compatibility, Radio Receivers, Telecommunication Circuits, Microwave Engineering and Information Theory. He has served as a course facilitator for the Institute of Distance Learning and has written the course books in Electromagnetic Field Theory and Information Theory. Positions he has occupied in the faculty include Examination Officer, Postgraduate Programs Coordinator and Vacation Training Officer.

Raymond Gyaang earned his BSc. Degree in Computer Science and Engineering from the University of Mines and Technology (UMaT), Tarkwa, Ghana, in 2014. Subsequently, he pursued an MEng. degree in Mobile Convergence Engineering from Hanbat National University (HNU), South Korea, graduating in 2020. Currently, he is dedicated to his PhD. studies in Telecommunication Engineering at Kwame Nkrumah University of Science and Technology (KNUST) in Ghana.
His current PhD research revolves around the design and implementation of a Dynamic Phase Six Port Network.